

HARDWARE USER MANUAL

MODEL 3165

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CAUTION
RISK OF ELECTRICAL SHOCK
DO NOT OPEN



This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.



If this instrument is to be powered from the AC line (mains) through an autotransformer, ensure the common connector is connected to the neutral (earth pole) of the power supply.



Before operating the unit, ensure the conductor (green wire) is connected to the ground (earth) conductor of the power outlet. Do not use a two-conductor extension cord or a three-prong/two-prong adapter. This will defeat the protective feature of the third conductor in the power cord.



Maintenance and calibration procedures sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures and heed warnings to avoid “live” circuit points.

Before operating this instrument:

1. Ensure the proper fuse is in place for the power source to operate.
2. Ensure all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If the instrument:

- fails to operate satisfactorily
- shows visible damage
- has been stored under unfavorable conditions
- has sustained stress

Do not operate until performance is checked by qualified personnel.

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Introduction

The Racal Instruments' Model 3165 (980899-001) is a dual-channel PXI-based Arbitrary Waveform Generator (AWG). The AWG is based on dual 14-bit high speed digital to analog converters. Figure 1 shows the functional block diagram for the 3165. As shown in the diagram channel-B is an exact copy of channel-A except for the addition of the signal path from channel-A. On the left of the diagram is the PXI Bus interface with all the required signals. The onboard stimulus generator contains an address counter and a 14bit x 512k RAM memory.

When the 3165 is triggered, the stimulus memory starts from its start address. During the measurement an internal or external clock increments the memory counter. When the counter reaches the value of the stop address it jumps back to the start address. This allows the generation of continues analog patterns.

If desired the generated analog signal can be filtered to remove quantization noise and improve the dynamic performance.

The attenuator has 7 steps of 3dB each. Since the Main DAC has a programmable reference voltage that allows a proportional output level variation of 3 dB, the Main DAC output level is proportionally adjustable over a range of 24dB.

A DC-offset voltage can be added to the signal before it is output via the differential 50 Ohm output stage.

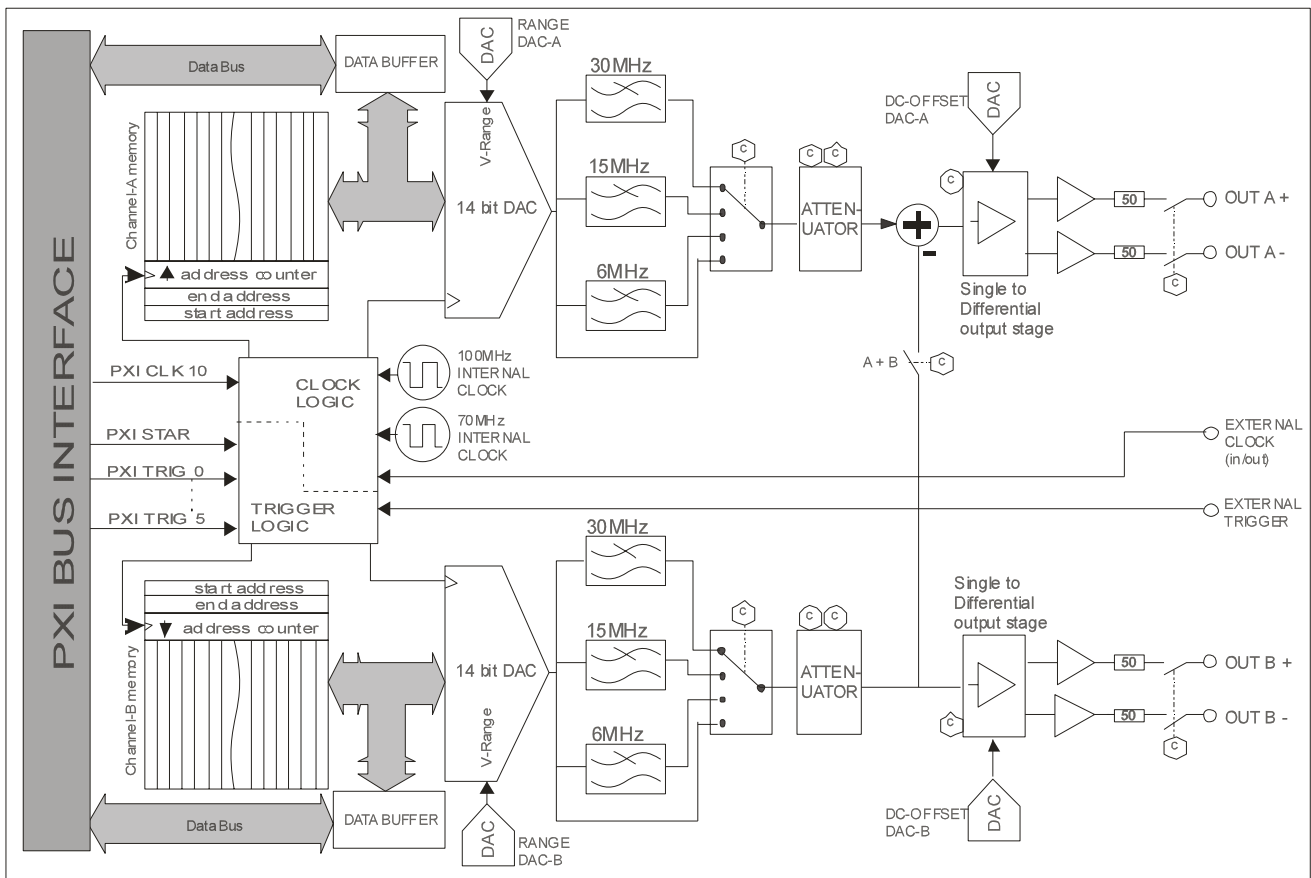


Figure 1 3165 Functional Block Diagram

1 Device Operation

1.1 Memory Operation

The stimulus memory of the 3165 is addressed through a counter. This counter is active during pattern generation as during reading or writing the memory via the bus. In Pattern generation mode the counter starts counting from the start (see table below) and increments on each sample clock until it reaches the end address. Then it jumps back to the start address and repeats the same memory segment. The start address and end address values should be written to the appropriate registers before the pattern starts. When writing the start address, this value is also loaded into the counter.

In bus access mode the same mechanism is active except that the clock is now a read or write signal. To write a memory section the start address and stop address should be set first. The counter is now pointing to the start address and the content of this address can be read or written via register 04 Hex (84 Hex). After each read or write the counter increments to the next address allowing burst read or write actions. Note that the counter will jump back to the start address when it reaches the stop address.

Since the memory may not be read or written during pattern generation, there is a Lock bit that should be set to allow pattern generation. The memory is then locked for reading or writing. This is possible again after setting the lock bit to unlock. A pattern that was still running at that moment will be aborted.

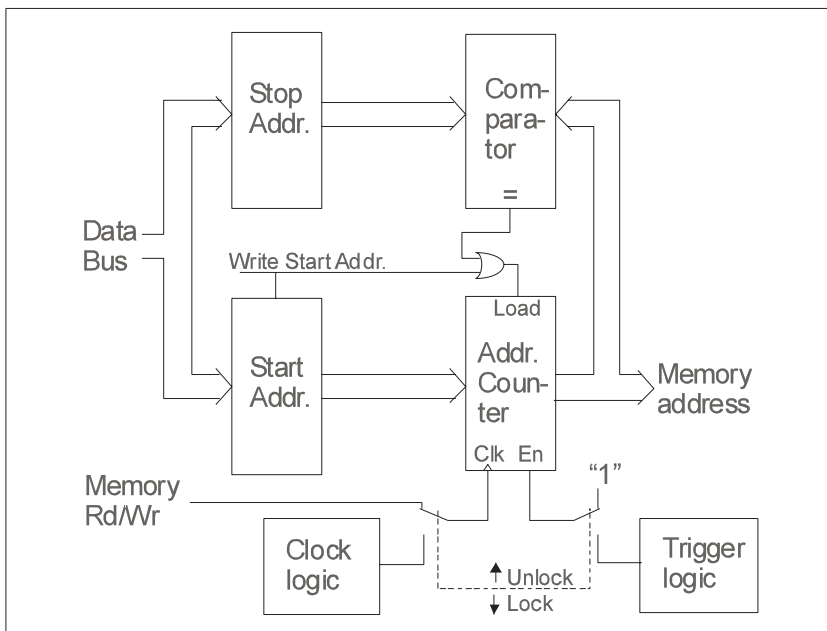


Figure 2

Register assignment:

ADDRESS Channel A (B)	Operation (R/W)	Data	Description
01 (81) Hex	W	00000 : 3FFFF Hex	Write stop address
02 (82) Hex	W	00000 : 3FFFF Hex	Write start address
04 (84) Hex	R and W	0000 : FFFF Hex (auto increment)	Read or write to memory
05 (85) Hex	R	00000 : 3FFFF Hex	Read counter
0F (8F) Hex	W	00 Hex Unlock 01 Hex Lock, ready for trigger	Lock / Unlock (Measurement mode / Memory access mode)

1.2 Trigger Processing

The 3165 starts generating a signal after it is triggered. The separate trigger circuits for Channel-A and Channel-B allows each channel to start on different sources and on different edges. The 3165 accepts triggers from the PXI back plane trigger sources including PXI_TRG[0:5] and PXI_STAR. In addition, the 3165 allows selection of the front panel trigger input and a software initiated trigger. The front panel trigger input uses normal TTL logic levels, with a 0.5V nominal threshold for a low level and a 2V nominal threshold for a high level. The 3165 can handle positive and negative, edge and level trigger signals, see the (SELECT TRIGGER EDGE) command. In Level trigger mode the pattern generator starts when Trigger goes active and stops when trigger goes inactive. In edge trigger mode the pattern generator starts at a trigger edge and either stops on the next trigger edge or runs continuously until stopped by the software. Figure 3 shows a diagram of the 3165 trigger processing.

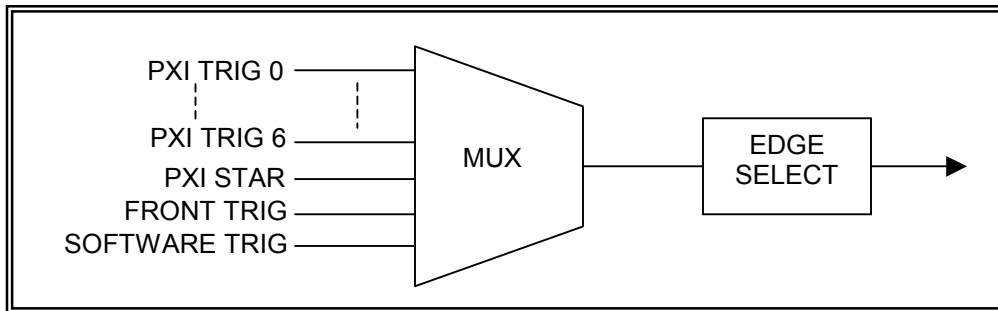


Figure 3

Register assignment:

ADDRESS Channel A (B)	Operation (R/W)	Data	Description
0B (8B) HEX	W	x0 Hex FRONT PANEL TRIG x1 Hex PXI TRIG 0 x2 Hex PXI TRIG 1 x3 Hex PXI TRIG 2 x4 Hex PXI TRIG 3 x5 Hex PXI TRIG 4 x6 Hex PXI TRIG 5 x7 Hex PXI STAR x8 Hex SOFTWARE TRIG	Select Trigger source
0B (8B) HEX	W	0x Hex positive level 1x Hex negative level 2x Hex positive edge, toggle on/off 3x Hex negative edge, toggle on/off 6x Hex positive edge, continuous 7x Hex negative edge, continuous	Select Edge

ADDRESS Channel A (B)	Operation (R/W)	Data	Description
07 (87) Hex	R and W	00 Hex No trigger 01 Hex Software trigger channel A 02 Hex Software trigger channel B 03 Hex Software trigger channel A & B	Write = software trigger start. Read = hardware and software trigger status.

1.3 Clock Select

After triggering, the memory counter runs on an internal or external clock signal. The external clock can be the front panel clock or the 10 MHz PXI clock. The two internal clock sources are either 100MHz and 70MHz. To run on lower clock frequencies it is possible to divide the clock source to a lower frequency with the onboard divider. The divider is 8 bit so it can divide with a maximum of 256. Both channels can be set to a different clock source and a different divider ratio. If the front panel clock input is not used by one of the two channels, the sample clock from channel-A is present on this connector. The front panel clock input has a 50 Ohm termination to ground.

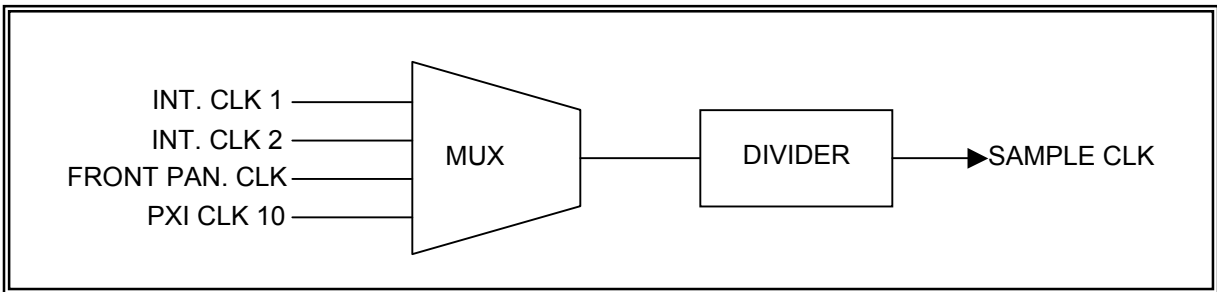


Figure 4

Register assignment:

ADDRESS Channel A (B)	Operation (R/W)	Data	Description
08 (88) HEX	W	00 Hex FRONT PANEL CLK 01 Hex INT CLK 1 (100MHz) 02 Hex INT CLK 2 (70MHz) 03 Hex PXI 10MHz CLK	Select Clock source
06 (86) HEX	W	00 : FF HEX	Write clock divider

1.4 Filter Select

The 3165 has a bank of selectable 3-pole low pass filters for each channel. These filters allows improved reconstruction of the analog output signal. The cutoff frequencies are: 6 MHz, 15 MHz, and 30 MHz. The filters can also be bypassed for reproduction of wide band signals.

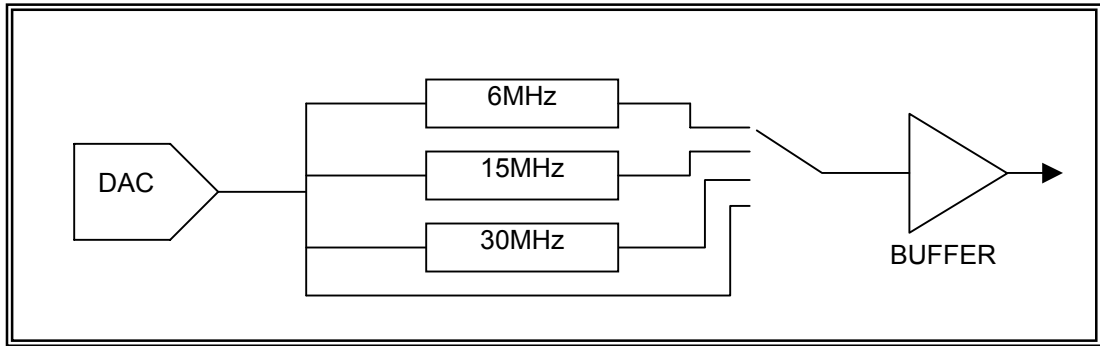


Figure 5

Register assignment:

ADDRESS Channel A (B)	Operation (R/W)	Data	Description
0A (8A) HEX	R and W	01 Hex No filter 02 Hex 6MHz filter 04 Hex 15MHz filter 08 Hex 30MHz filter	Select Filter DAC A

1.5 Output Stage

Both channels have two different connect modes, single and differential output. If the analog output is disconnected, the internal circuit is disconnected from the output by a mechanical switch. The output includes a series 50Ω 0.1% tolerance resistor as back termination.

It is also possible to add both channels together.

Pay attention, the addition is $A + (B \text{ inverted})$.

If the signal from DAC B is added to Channel A, the signal from DAC B is still present on channel B.

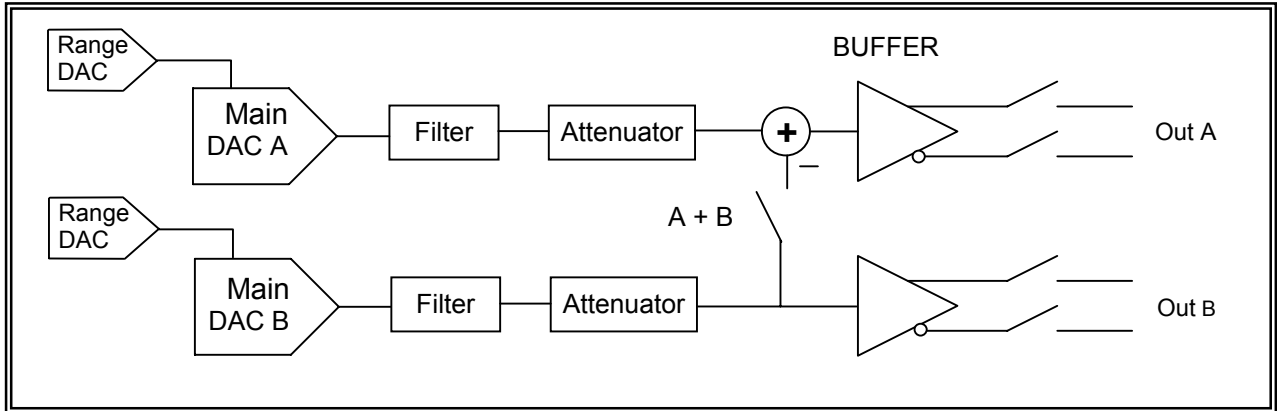


Figure 6

Register assignment:

ADDRESS Channel A (B)	Operation (R/W)	Data (*)	Description
09 (89) HEX	R and W	40 Hex single out (OUT+) 60 Hex differential out C0 Hex Add B to A single out E0 Hex Add B to A diff out	Output single/ differential Output add (only for channel-A)

(*) bits should be OR-ed with the attenuator code to obtain the Hex code to be written

1.6 DAC Range

The output signal level is a combination of the DAC, who sets the reference from the main DAC, and the attenuator (described in part 1.7). The attenuator has steps of -3dB, and the range DAC covers the range values in-between. The DAC is serial programmed through a 3-wire serial bus that accepts 16-bit serial words. Data is loaded MSB first. Data is shifted into the serial input on the rising edge of clock. After transferring data chip select must be taken low so that the DAC reacts on the data. The serial data must be written through the parallel data lines from the module. For connections and a timing diagram see "Offset DAC" description.

Register assignment:

ADDRESS Channel A (B)	Operation (R/W)	Data	Description
0D Hex	W	0000 : FFFF (bit0=DO bit1=CLK bit3=OFFCS bit4=RANGECS)	Write range DAC & offset DAC

1.7 Attenuator

The output level can be attenuated from 0 to -21dB in steps of -3dB

For ranging steps less then 3dB, see DAC Range description.

Register assignment:

ADDRESS Channel A (B)	Operation (R/W)	Data (*)	Description
09 (89) HEX	W	01 Hex 0dB 11 Hex - 3dB 02 Hex - 6dB 12 Hex - 9dB 04 Hex -12dB 14 Hex -15dB 08 Hex -18dB 18 Hex -21dB	Select Attenuation (bits should be OR-ed with the output mode bit to obtain the Hex code to be written)

(*) bits should be OR-ed with the output stage configuration to obtain the Hex code to be written

1.8 DAC Offset

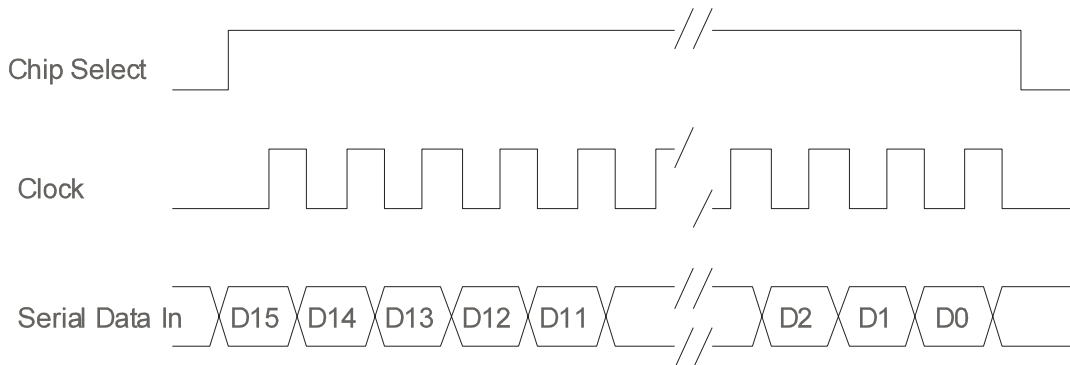
It is possible to add a DC offset to the output signal with the offset DAC. The offset DAC is serial programmed through a 3-wire serial bus that accepts 16-bit serial words. Data is loaded MSB first. Data is shifted into the serial input on the rising edge of clock. After transferring data chip select must be taken low so that the DAC reacts on the data. The serial data must be written through the parallel data lines from the module. For connections see Table 1

Register assignment:

ADDRESS Channel A (B)	Operation (R/W)	Data	Description
0D Hex	W	0000 : FFFF (bit0=DO bit1=CLK bit3=OFFCS bit4=RANGECS)	Write range DAC & offset DAC

Data line	Serial function
D0	Serial data in
D1	clock
D3	chip select offset DAC
D4	chip select range DAC

Table 1 Serial DAC control line assignment



Serial DAC timing diagram

1.9 Output Offset Calibration DAC

To minimize the total output offset and differential offset, two calibration DACs are added. These 10 bit DACs insert a calibration voltage to the output buffer. (figure 7) The calibration can be done with calibration software. After calibration the settings are stored in the on-board EEprom
It is recommended to start a calibration after a system warm up period of half an hour.
 The calibration details and the EEprom organization can be found in the calibration manual.
 For connections and register assignment see "Offset correction DAC" description

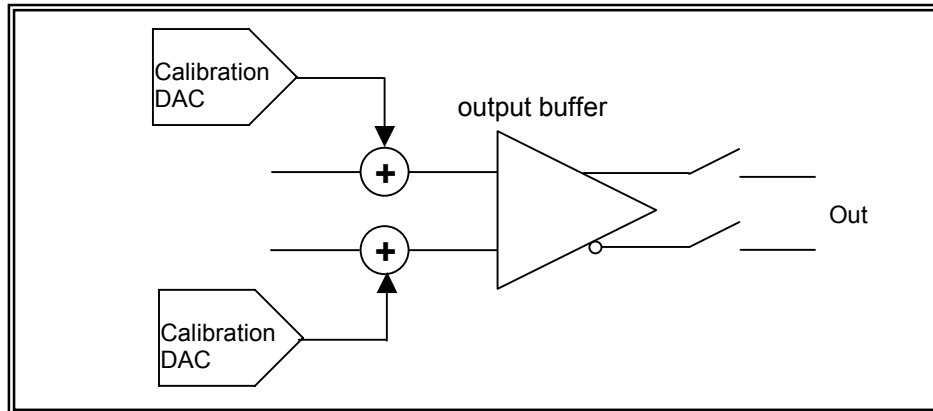


Figure 7

The output calibration DAC's are all in one chip. To select the offset calibration DAC for each output, an address is added to the input code (see Figure 8). For connections see "Offset Correction DAC" description.

offset calibration	Address
+ out Channel A	8 hex
- out Channel A	7 hex
+ out Channel B	1 hex
- out channel B	0 hex

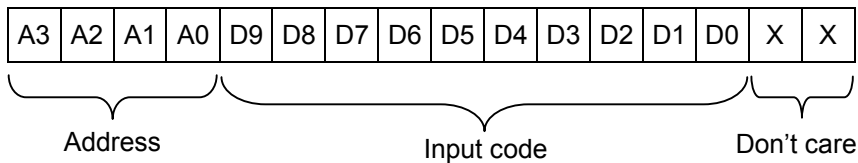


Figure 8

1.10 Offset Correction DAC

This calibration DAC is a offset correction for the main DAC. If this DAC is calibrated the output must stay stable with all settings from the range DAC.

To calibrate this DAC, the signal DAC should be programmed midscale (code 8000 hex) The offset correction DAC should now be trimmed in such a way that the voltage on the output does not change when the range DAC is changed over the full range.

The calibration software automatically sets all the DACs in the right position. All details can be found in the calibration manual.

Register assignment:

ADDRESS Channel A (B)	Operation (R/W)	Data	Description
0E Hex	W	0000 : FFFF (bit0=DO bit1=CLK bit3=cal-offcorCS bit4=cal-offoutCS)	Write Calibration offset Zero scale from DAC and output offset (10bit)

Data line	Serial function
D0	Serial data in
D1	clock
D3	chip select offset correction DAC
D4	chip select output offset calibrationDAC

Table 2 Serial Calibration DAC Control Line Assignment

1.11 Memory Segmentation

On the 3165 there is a 512k words stimulus memory for each channel. In this memory the wave forms can be stored. Its also possible to split up the memory in smaller segments, and load different waveforms into individual segments. The desired signal can be selected with the start and stop address. When the 3165 is running the waveform stored in that memory segment is converted by the DAC to the analog output signal. It is not possible to change from memory segment while the DAC is running.

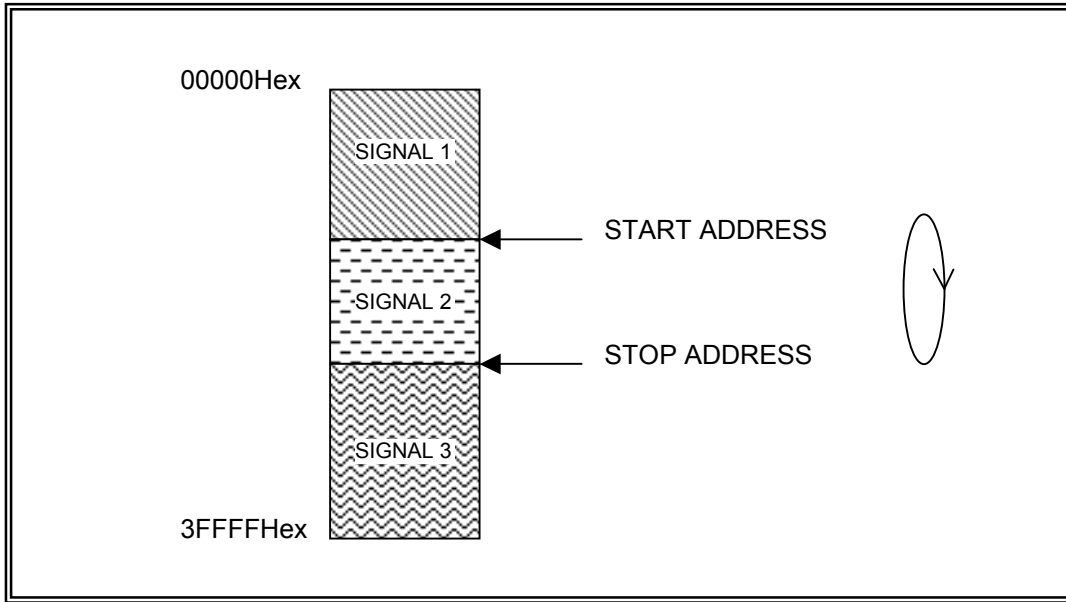


Figure 9

Register assignment:

ADDRESS Channel A (B)	Operation (R/W)	Range	Description
02 (82) HEX	W	00000 : 3FFFF HEX	Write start address
01 (81) HEX	W	00000 : 3FFFF HEX	Write stop address

1.12 Serial EEPROM

The 3165 has a 93C66 serial EEPROM onboard (256 locations of 16 bit each). This EEPROM is used to store calibration values and other module specific information.

The read and write sequence for the EEPROM are according the Microwire® standard. Table 2 shows the bit assignment. There is only one EEPROM for both channels! Access to the EEPROM is via the Channel-A register bank only.

Register assignment:

ADDRESS	Operation (R/W)	Range	Description
0C Hex	R and W	00 : FF Hex	Read Write EEPROM

Data line	Serial function
D0	Serial data in/out
D1	clock
D3	chip select

Table 3 Serial EEPROM Control Line Assignment

2 Front Panel

A diagram of the 3165 front panel is shown in Figure 10. On the front panel, there are six SMB coaxial connectors. Four connectors are used for the differential output from channel A and B. The two other connectors are for the trigger input and the clock. The function of these connectors is described below.

OUT A+ and OUT A-

This is the output from channel A. In single ended mode the connector A+ is used. In differential mode the output signal is present between A+ and A-. The output impedance is always 50Ω.

OUT B+ and OUT B-

This is the output from channel B. In single ended mode the connector B+ is used. In differential mode the output signal is present between B+ and B-. The output impedance is always 50Ω.

CLK in/out

This connector is bi-directional. If the clock source selector is set to FRONT this connector is an input for the sample clock, in all other clock source modes this connector is an output for the sample clock. This signal can be used to clock or synchronize other modules. The input impedance of this input is 50Ω.

TRIG in

If the trigger selector is set to FRONT this input accepts signals that starts generation of output waveforms. The trigger input can be set to level or negative level trigger and edge or negative edge trigger. Trigger level for this input is TTL.

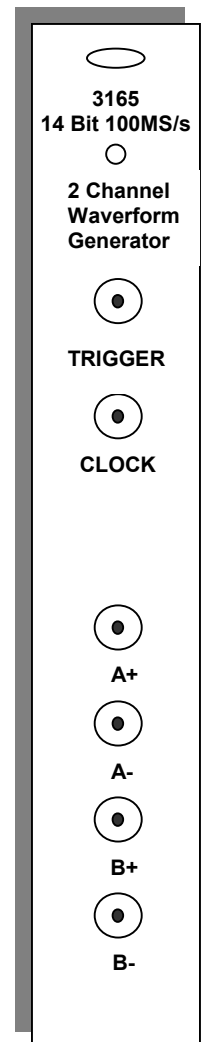


Figure 10

3 PXI Interface

Supplied with the 3165 is a PC software package that consists of a windows driver, Labview driver and a demo program. Details on how to use this software are given in the 3165 Software User Manual (980899-002).

APPENDIX A

Register assignment:

Channel-A

ADDRESS	Operation (R/W)	DATA	Description
00 Hex	W	XXXX	Set counter to start address
01 Hex	W	00000 : 7FFFF Hex	Write stop address
02 Hex	W	00000 : 7FFFF Hex	Write start address
03 Hex	W	0000 : 3FFF Hex	Write direct to DAC A
04 Hex	R and W	0000 : FFFF Hex (auto increment)	Read or write to memory
05 Hex	R	00000 : 7FFFF Hex	Read counter
06 Hex	W	00 : FF	Write clock divider
07 Hex	R and W	00 Hex No trigger 01 Hex Software trigger channel A 02 Hex Software trigger channel B 03 Hex Software trigger channel A & B	Write = software trigger start. Read = hardware and software trigger status.
08 Hex	W	00 Hex FRONT PANEL CLK 01 Hex INT CLK 1 (100MHz) 02 Hex INT CLK 2 (70MHz) 03 Hex PXI 10MHz CLK 10 Hex Front clock out enable	Select Clock source
09 Hex	R and W	01 Hex 0dB 11 Hex -3dB 02 Hex -6dB 12 Hex -9dB 04 Hex -12dB 14 Hex -15dB 08 Hex -18dB 18 Hex -21dB	Select Attenuator (Combine with Analog output select code)
09 Hex	R and W	40 Hex Single output (OUT+) 60 Hex Differential output C0 Hex add B to A single out E0 Hex add B to A differential out	Analog output select (Combine with Attenuator select code)
0A Hex	R and W	01 Hex No filter 02 Hex 6MHz filter 04 Hex 15MHz filter 08 Hex 30MHz filter	Select Filter
0B Hex	W	x0 Hex FRONT PANEL TRIG x1 Hex PXI TRIG 0 x2 Hex PXI TRIG 1 x3 Hex PXI TRIG 2 x4 Hex PXI TRIG 3 x5 Hex PXI TRIG 4 x6 Hex PXI TRIG 5 x7 Hex PXI STAR x8 Hex SOFTWARE TRIG	Select Trigger source (Combine with select Edge code)
0B Hex	W	0x Hex positive level 1x Hex negative level 2x Hex positive edge, toggle on/off 3x Hex negative edge, toggle on/off 6x Hex positive edge, continuous 7x Hex negative edge, continuous	Select Edge
0C Hex	R and W	00 : FF Hex bit0=DO/Di bit1=CLK bit3=CS	Read / Write EEPROM
0D Hex	W	0000 : FFFF (bit0=DO bit1=CLK bit3=OFFCS bit4=RANGECS)	Write range DAC & output offset DAC (both 16 bit)
0E Hex	W	bit0=DO bit1=CLK bit3=cal-offcorCS bit4=cal-offoutCS 7 Hex = - output 8 Hex = + output	Write offset correction DAC(12bit) and differential output offset calibration DAC(10bit)
0F Hex	W	00 Hex Unlock 01 Hex Lock, ready for trigger	Lock / Unlock (Measurement mode / Memory access mode)

Channel-B

ADDRESS	Operation (R/W)	DATA	Description
80 Hex	W	XXXX	Set counter to start address
81 Hex	W	00000 : 3FFFF Hex	Write stop address
82 Hex	W	00000 : 3FFFF Hex	Write start address
83 Hex	W	0000 : 3FFF Hex	Write direct to DAC A
84 Hex	R and W	0000 : FFFF Hex (auto increment)	Read or write to memory
85 Hex	R and W	00000 : 3FFFF Hex	Read counter & Set counter to start address
86 Hex	W	00 : FF	Write clock divider
87 Hex	R and W	00 Hex No trigger 01 Hex Software trigger channel A 02 Hex Software trigger channel B 03 Hex Software trigger channel A & B	Write = software trigger start. Read = hardware and software trigger status.
88 Hex	W	00 Hex FRONT PANEL CLK 01 Hex INT CLK 1 (100MHz) 02 Hex INT CLK 2 (70MHz) 03 Hex PXI 10MHz CLK 10 Hex Front clock out enable	Select Clock source
89 Hex	R and W	01 Hex 0dB 11 Hex - 3dB 02 Hex - 6dB 12 Hex - 9dB 04 Hex -12dB 14 Hex -15dB 08 Hex -18dB 18 Hex -21dB	Select Attenuator (Combine with Analog output select code)
89 Hex	R and W	40 Hex Single output (OUT+) 60 Hex Differential output C0 Hex add B to A single out E0 Hex add B to A differential out	Analog output select (Combine with Attenuator select code)
8A Hex	R and W	01 Hex No filter 02 Hex 6MHz filter 04 Hex 15MHz filter 08 Hex 30MHz filter	Select Filter
8B Hex	W	x0 Hex FRONT PANEL TRIG x1 Hex PXI TRIG 0 x2 Hex PXI TRIG 1 x3 Hex PXI TRIG 2 x4 Hex PXI TRIG 3 x5 Hex PXI TRIG 4 x6 Hex PXI TRIG 5 x7 Hex PXI STAR x8 Hex SOFTWARE TRIG	Select Trigger source (Combine with select Edge code)
8B Hex	W	0x Hex positive level 1x Hex negative level 2x Hex positive edge, toggle on/off 3x Hex negative edge, toggle on/off 6x Hex positive edge, continuous 7x Hex negative edge, continuous	Select Edge
8C Hex	R and W	00 : FF Hex bit0=DO/Di bit1=CLK bit3=CS	Read / Write EEPROM
8D Hex	W	0000 : FFFF (bit0=DO bit1=CLK bit3=OFFCS bit4=RANGECS)	Write range DAC & output offset DAC (both 16 bit)
8E Hex	W	bit0=DO bit1=CLK bit3=cal-offcorCS bit4=cal-offoutCS 1Hex = - output 2 Hex = + output	Write offset correction DAC(12bit) and differential output offset calibration DAC(10bit)
8F Hex	W	00 Hex Unlock 01 Hex Lock, ready for trigger	Lock / Unlock (Measurement mode / Memory access mode)

4 Specifications

Typical 22°C

General:

Number of channels..... 2
 DAC resolution..... 14 bit
 Update rate..... DC- 100MHz
 Memory depth..... 512k per channel

Analog:

output configuration..... Differential or single ended
 output ranges..... 350mVpp - 5Vpp proportional into open circuit
 output impedance..... 50Ω
 output coupling..... DC
 DC output offset range..... -2.5 Volt to +2.5Volt
 Output filters..... None, 6MHz, 15MHz, 30MHz (3-pole Butterworth)
 Bandwidth (-3dB) no filter.....
 Channel crosstalk..... <80dB at 1MHz
 Frequency response, referenced at 500kHz (no filter)
 Absolute accuracy..... ±(500μV+0.1% of range)
 Relative accuracy (INL)..... ±0.025% of range
 SFDR (fs = 100MHz/ Vout = 2Vpp)..... 78dB @ f-out = 1MHz
 64dB @ f-out = 10MHz
 SINAD (fs = 100MHz/ Vout = 2Vpp)..... 65dB @ f-out = 1MHz
 62dB @ f-out = 10MHz

Sample clock:

Clock sources..... Internal, external and PXI 10MHz

Internal clock:

Internal clock frequency..... 50MHz and 70MHz dividable by 1 to 256
 clock accuracy..... 50MHz and 70MHz ±100ppm

External clock input:

External clock source..... SMB connector front
 Maximum external clock frequency..... 100 MHz dividable by 1 to 256
 External clock levels..... Vlow < 0.6V Vhigh > 1.4Volt
 External clock impedance..... 50Ω DC

External clock output:

Clock output impedance..... 50Ω DC
 Clock output levels..... Vlow < 0.6V Vhigh > 4.5Volt (no load)

Triggering:

Trigger sources..... Front, PXI trigger 0...5, PXI star trigger, software trigger
 Trigger modes..... Positive level, negative level, positive edge, negative edge, positive edge continuous and negative edge continuous
 Front trigger impedance..... 10kΩ DC
 Front trigger levels..... Vlow < 0.6V Vhigh > 2.4Volt

Power Requirements:

	+3.3V	+5V	+12V	-12V
maximum power consumption.....	250mA	700mA	240mA	240mA

Environment:

Operating temperature..... 0 to 50°C
 Storage temperature..... 0 to 70°C
 Relative humidity..... 10 to 80 %, non-condensing

Mechanical

Size..... Single slot, 3u high (100mm x 160mm)
 Weight..... 210 gram

Product Support

Racal Instruments has a complete Service and Parts Department. If you need technical assistance or should it be necessary to return your product for repair or calibration, call 1-800-722-3262. If parts are required to repair the product at your facility, call 1-949-859-8999 and ask for the Parts Department.

When sending your instrument in for repair, complete the form in the back of this manual.

For worldwide support and the office closes to your facility, refer to the Support Offices section on the following page.

Warranty

Use the original packing material when returning the 3165 (980899-001) to Racal Instruments for calibration or servicing. The original shipping container and associated packaging material will provide the necessary protection for safe reshipment.

If the original packing material is unavailable, contact Racal Instruments Customer Service for information.

Support Offices

RACAL INSTRUMENTS

United States

(Corporate Headquarters and Service Center)
4 Goodyear Street, Irvine, CA 92618
Tel: (800) 722-2528, (949) 859-8999; Fax: (949) 859-7139

5730 Northwest Parkway Suite 700, San Antonio, TX 78249
Tel: (210) 699-6799; Fax: (210) 699-8857

Europe

(European Headquarters and Service Center)
18 Avenue Dutartre, 78150 LeChesnay, France
Tel: +33 (0)1 39 23 22 22; Fax: +33 (0)1 39 23 22 25

29-31 Cobham Road, Wimborne, Dorset BH21 7PF, United Kingdom
Tel: +44 (0) 1202 872800; Fax: +44 (0) 1202 870810

Via Milazzo 25, 20092 Cinisello B, Milan, Italy
Tel: +39 (0)2 6123 901; Fax: +39 (0)2 6129 3606

Technologie Park, Friedrich Ebert Strasse, 51429 Bergisch Gladbach,
Germany
Tel: +49 (0) 2204 844200; Fax: +49 (0) 2204 844219

REPAIR AND CALIBRATION REQUEST FORM

To allow us to better understand your repair requests, we suggest you use the following outline when calling and include a copy with your instrument to be sent to the Racal Instruments Repair Facility.

Model _____ Serial No. _____ Date _____

Company Name _____ Purchase Order # _____

Billing Address _____
City _____

State/Province _____ Zip/Postal Code _____ Country _____

Shipping Address _____
City _____

State/Province _____ Zip/Postal Code _____ Country _____

Technical Contact _____ Phone Number () _____

Purchasing Contact _____ Phone Number () _____

1. Describe, in detail, the problem and symptoms you are having. Please include all set up details, such as input/output levels, frequencies, waveform details, etc.

2. If problem is occurring when unit is in remote, please list the program strings used and the controller type.

3. Please give any additional information you feel would be beneficial in facilitating a faster repair time (i.e., modifications, etc.)

4. Is calibration data required? Yes No (please circle one)
Call before shipping Ship instruments to nearest support office.

Note: We do not accept
"collect" shipments